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COMMUNICATION TIMING COORDINATION TECHNIQUES

BACKGROUND OF THE INVENTION

[0001] This invention relates to digital telephony and more specifically relates to coordinating the transmission of data in digital telephony.

[0002] Digital telephony, the transmission of voice over digital communications systems, requires coordination of a head end unit to a remote unit. However, the reference clocks at the head end unit and remote unit are, in general, produced from asynchronous sources. For example, the reference clocks at both the head end unit and remote unit may be generated by local crystal oscillators, each of

which is free running. Due to manufacturing uncertainties, the frequencies of these two oscillators (and correspondingly the head end unit and remote unit reference clocks) will not match.

[0003] There is typically a frequency offset of several hundred parts per million (ppm) between the head end clock and remote clock. In addition to a constant offset, there is the possibility of jitter on either of the generated clocks. Hence, the head end unit (also called the central office, or CO) operates at a different frequency than the remote unit (sometimes referred to as the customer premises equipment, or CPE). The frequency offset and jitter interfere with proper communication of data.

[0004] In the past, the frequency offset between the head end and remote clocks has been handled by sending both voice and non-voice data in flagged packets. Many of the packets include no voice data. The packets with both voice and non-voice data are sent with a prefix or flag that indicates the presence of voice data. In response to the flag, the receiving unit switches the voice data to a voice

data buffer memory. After some voice data has been stored in the buffer memory, it is processed by voice processing circuitry. The use of a flag to indicate the presence of voice data reduces the bandwidth available for data transmission. The processing required to handle the voice data in response to the flags requires delays and expensive processing equipment. This invention addresses these problems and provides a solution.

[0005] U.S. Patent Number 5,479,457 (Dec. 26, 1995) describes clock smoothing. However, it does not teach any clock relationships between a central office and customer premises equipment.

[0006] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF SUMMARY OF THE INVENTION

[0007] An exemplary apparatus form of the invention is useful in a communication unit for sending transmit data. In such an environment, the unit comprises a receiver arranged to recover input data transmitted at a first transfer rate in response to a first transmit clock signal and a transmitter arranged to transmit the transmit data at a second transfer rate in response to a second transmit clock signal coordinated with the first transmit clock signal. The second transmit clock signal comprises a frequency defined at least in part by a predetermined relationship between the first transfer rate and second transfer rate.

[0008] An exemplary method form of the invention is useful for sending transmit data. In such an environment, the method comprises recovering input data transmitted at a first transfer rate in response to a first transmit clock signal. A second transmit clock signal is generated and coordinated with the first transmit clock signal. The transmit data is transmitted in response to the second

transmit clock signal at a second transfer rate. The second transmit clock signal comprises a frequency defined at least in part by a predetermined relationship between the first transfer rate and second transfer rate.

[0009] By using the foregoing techniques, coordination between head end and remote communication units can be economically maintained with a degree of precision previously not available. No flags indicating the presence of packets with voice data are required. In addition, the complexity of the requisite processing circuitry is reduced.

[0010] These and other advantages and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a schematic block diagram of one form of a communication system embodying the invention, including a remote unit comprising a modulator.

[0012] Figure 2 is a flow diagram describing the operation of a portion of the apparatus in Figure 1.

[0013] Figure 3 is a schematic block diagram of the remote unit modulator shown in Figure 1.

[0014] Figure 4 is a flow diagram describing the operation of a portion of the apparatus shown in Figure 3.

[0015] Figure 5 is a flow diagram illustrating more detailed operation of one of the steps of operation shown in Figure 4.

[0016] Figure 6 is a schematic block diagram of additional details of the feedback circuit shown in Figure 3.

[0017] Figure 7 is a schematic block diagram of the frequency divider shown in Figure 6.

[0018] Figure 8 is a schematic block diagram of the phase detector shown in Figure 6.

[0019] Figure 9 is a schematic block diagram of the pre-filter shown in Figure 6.

[0020] Figure 10 is a schematic block diagram of loop filter shown in Figure 6.

[0021] Figure 11 is a schematic block diagram of the numeric controlled oscillator (NCO) shown in Figure 6.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Referring to Figure 1, one form of communication system in which the invention may be employed includes a digital subscriber line (DSL) system 5 employing discrete multitone modulation (DMT) or a single carrier modulation (QAM, CAP). Such a system includes a head end unit or central office 10 employing a transmitter 12 comprising a source of head end data 14, an encoder 16 and a modulator 18. A symbol clock 20 operates at a predetermined frequency to produce a symbol transmit clock signal on a conductor 21. Modulator 18 uses the symbol transmit clock signal to modulate the data originating at source 14 with DMT or single carrier modulation. The modulated data is transmitted at a downstream transfer rate, such as 5 megabits per second (Mb/s), through a hybrid circuit 22 and a DSL communication line 28 in a downstream direction D

(downstream data). The downstream transmitted data includes information about the symbol transmit clock signal. Line 28 comprises conventional telephone twisted pair conductors.

[0023] Head end unit 10 also employs a receiver 24 comprising a demodulator 26 and a decoder 27 that generates data transmitted to a utilization circuit (not shown).

[0024] A remote unit 30 employs a receiver 32 comprising a hybrid circuit 34, a demodulator 36 and a decoder 38 that generates data transmitted to a utilization circuit (not shown) in response to the received downstream data. Receiver 32 is a coherent receiver comprising an analog to digital converter (ADC) (not shown) and a loop algorithm that derives a control word (CW) from the received signal, which contains information about symbol transmit clock that is used to recover the symbol transmit clock signal generated by head end unit 10. Demodulator 36 generates a recovered clock signal RX_CLK on a conductor 37 by processing the signal received on line 28 with the downstream data from head end unit 10. The RX_CLK signal

is a reconstructed version of the symbol transmit clock signal generated by symbol clock 20.

[0025] Remote unit 30 also includes a transmitter 40 comprising a remote data source 42, an encoder 44 and a modulator 46 that receives the RX_CLK signal. Modulator 46 generates upstream remote transmit data that is sent through a conductor 47, hybrid circuit 34 and line 28 to head end unit 10 in an upstream direction U (upstream data). The remote transmit data is sent at an upstream transfer rate, such as 100 kilobits per second (Kb/s). Modulator 46 uses the RX_CLK signal to generate a remote transmit clock signal that is coordinated with the symbol transmit clock signal. The frequency of the remote transmit clock signal has a predetermined relationship between the downstream transfer rate in direction D and the upstream transfer rate in direction U. For example, the frequency of the remote transmit clock signal may be proportional to a ratio of the downstream transfer rate and the upstream transfer rate. The remote transmit clock signal is used by modulator 46 to generate the upstream transmit data that is sent to head end unit 10 in direction

U. The upstream remote transmit data also includes information about remote transmit clock signal.

[0026] The remote transmit data is received by hybrid circuit 22 and is sent to demodulator 26. The received signal is used by demodulator 26 to recover the remote transmit clock signal in the same manner that demodulator 36 recovers the symbol clock signal from the head end unit 10. The recovered signal is a reconstructed version of the remote transmit clock signal generated by modulator 46. As a result of this operation, the upstream data transmitted to head end unit 10 in the U direction can be demodulated and decoded with a degree of accuracy and economy previously unavailable. For example, no flags indicating packets with voice data are required.

[0027] Referring to Figure 2, the operation of remote unit 30 starts at step S50 and continues with step S51 in which input data transmitted at the downstream transfer rate in response to the symbol transmit clock signal on conductor 21 is recovered by receiver 32.

[0028] In step S52, modulator 46 generates a remote transmit clock signal that is coordinated with the symbol transmit clock signal on conductor 21.

[0029] In step S53, modulator 46 transmits remote transmit data in response to the remote transmit clock signal at the upstream transfer rate.

[0030] In step S54, modulator 46 defines the frequency of the remote transmit clock signal at least in part by a predetermined relationship between the downstream transfer rate and the upstream transfer rate. For example, the frequency can be determined at least in part by a ratio of the upstream transfer rate and the downstream transfer rate. The foregoing phase of the operation ends at step S55.

[0031] Referring to Figure 3, modulator 46 includes a clock generator 60 that generates clock signals TX_CLK and TX_FS. As an alternative embodiment, the circuitry and loop algorithm that generates clock signal RX_CLK also may be incorporated into clock generator 60.

[0032] A frequency divider 62 is arranged to alter the RX_CLK frequency by a ratio of the downstream transfer rate and the upstream transfer rate to generate a clock signal TX_CLK_CO. More specifically, the frequency of RX_CLK is multiplied by the quantity downstream transfer rate/upstream transfer rate to generate TX_CLK_CO.

[0033] The transmit data received from encoder 44 on conductor 45 is filtered by a transmit shaping filter 66, which "shapes" the transmit data so that it is appropriately band-limited for transmission. The filter may also be used to give the transmit data certain properties, e.g., it may filter the data to make it distortion-free.

[0034] A buffer memory 70 is arranged to write the filtered and processed transmit data to the buffer memory in response to the TX_CLK_CO clock signal on a write input 72 and is arranged to read the transmit data from the buffer memory in response to a transmit clock signal TX_CLKA on a read input 74.

[0035] An interpolator 80 interpolates the transmit data so that it is appropriate for an output unit 90 arranged to place the transmit data into a form suitable for transmission in response to a sample clock signal TX_FS operating at a sample rate of, for example, 20 MHz. The rate of the TX_CLKA signal may be, for example, only half the rate of the TX_FS signal. In general, the TX_CLKA and TX_FS signals are not synchronized.

[0036] Output unit 90 comprises a digital to analog converter (DAC). The digital data is sampled by sample clock signal TX_FS.

[0037] A feedback circuit 100 is arranged to generate the transmit clock signal TX_CLKA by filtering or smoothing the TX_CLK_CO clock signal and to generate phase information μ on a conductor 101 in response to the phase difference between the transmit clock signal TX_CLKA and the sample clock signal TX_FS to enable interpolation of the transmit data into a form suitable for output unit 90.

[0038] One mode of the operation of modulator 46 is described in Figure 4. The operation starts at step S110.

[0039] In step S112, downstream data is received from head end unit 10, including information about symbol transmit clock generated on conductor 21. In step S114, demodulator 36 generates a recovered symbol clock signal RX_CLK from the symbol clock information.

[0040] In step S116, a rate-altered clock signal (TX_CLK_CO) is generated by altering the frequency of RX_CLK by a ratio of the upstream transfer rate and the downstream transfer rate.

[0041] In step S118, an upstream transmit clock signal (TX_CLKA) is generated by filtering or smoothing of the rate-altered clock signal.

[0042] In step S120, the upstream transmit data is stored in response to the rate-altered clock signal.

[0043] In step S122, the upstream transmit data is read in response to the upstream transmit clock (TX_CLKA).

[0044] In step S124, the upstream transmit data is placed in a form suitable for transmission to head end unit

10 in response to a sample clock signal (TX_FS) operating at a sample rate.

[0045] In step S126, phase information is generated in response to the phase difference between the upstream transmit clock signal (TX_CLKA) and the sample clock signal (TX_FS). This mode of the operation ends at step S128.

[0046] Figure 5 illustrates additional details about the operation of step S118 shown in Figure 4. The operation starts with step S130 and continues with step S132 in which the repetition rate (or frequency) of the rate-altered signal TX_CLK_CO is compared to the repetition rate (or frequency) of the upstream transmit clock TX_CLKA.

[0047] In step S134, if the repetition rate of TX_CLK_CO is less than the repetition rate of TX_CLKA, the repetition rate of TX_CLKA is decreased.

[0048] In step S136, if the repetition rate of TX_CLK_CO is greater than the repetition rate of TX_CLKA, the repetition rate of TX_CLKA is increased.

[0049] In step S138, if the repetition rate of TX_CLK_CO is substantially the same as the repetition rate of TX_CLKA, the repetition rate of TX_CLKA is left unchanged. This mode of operation then ends at step S140

[0050] Additional details about the embodiment shown in Figures 1 and 3 are provided in the following paragraphs.

[0051] The embodiment relies on the availability of an upstream transmit clock, such as TX_CLKA, at remote unit 30 that is coordinated with the symbol transmit clock of head end unit 10. The upstream transmit clock can be generated in any number of ways, and can be obtained easily under the assumption that receiver 32 is a coherent receiver. In digital telephony, receiver 32 typically recovers the head end unit 10 symbol transmit clock. This recovered symbol clock (RX_CLK) may be "locked" to the symbol transmit clock 20, and can therefore be used to generate a suitable upstream transmitter clock at remote unit 30 (e.g., by means of clock multiplication or division) which will itself be "locked" to symbol transmit clock 20. However, the recovered clock (RX_CLK) has two undesirable character-

istics: 1) it is bursty (non-uniform) and 2) it is in the receiver 32 clock domain, whereas the upstream transmitter clock must be in the transmitter 40 clock domain. These issues are addressed below.

[0052] Figure 3 is a schematic block diagram of an exemplary circuit for generating an upstream transmitter clock (TX_CLKA) that is "locked" to the recovered symbol clock (RX_CLK). RX_CLK is used to create a rate-altered clock signal (TX_CLK_CO) by means of circuit 148 (Figure 6). However, TX_CLK_CO is in the receiver 32 clock domain (RX_CLK), whereas upstream transmitter data must be in the transmitter 40 clock domain (TX_FS, or the output unit clock). Hence, data must be transferred from the RX_CLK domain (TX_CLK_CO) into the TX_FS domain. This is done by creating an additional clock signal, TX_CLKA, which is also "locked" to the rate altered signal TX_CLK_CO. Another characteristic of TX_CLKA is that it contains the phase information (μ) needed to interpolate the upstream data transmit signal to the output unit sample clock (TX_FS).

[0053] The embodiment shown in Figure 3 uses two components to synchronize the clocks: a digital phase locked loop (PLL) shown in Figure 6 and incorporated into feedback circuit 100 (Figure 3), and a frequency divider 62 (Figure 3). The frequency divider divides the repetition rate of RX_CLK by the ratio of the downstream transfer rate to the upstream transfer rate in order to generate rate-altered signal TX_CLK_CO. RX_CLK is "synchronized" to the symbol clock 20 signal by making use of the clock recovery in receiver 32. The average clock repetition rate or frequency of TX_CLK_CO is thereby "locked" to the symbol clock 20 signal. However, the rate-altered signal is bursty and noisy. The digital PLL in feedback circuit 100 is used to generate a clean upstream transmit clock signal (TX_CLKA).

[0054] Referring to Figure 3, buffer memory 70 is a first in first out (FIFO) that guarantees a safe hand-off between the two different clock domains and proper timing coordination. Theoretically, the FIFO 70 can be placed in various locations in transmitter 40 and for this embodiment, there is no restriction on the location.

However, by placing FIFO 70 in front of interpolator 80, phase information μ can be immediately used. In this embodiment interpolator 80 comprises a Variable Interpolator / Decimator (VID). The size of FIFO 70 can be determined by analyzing the burstiness of the rate-altered clock signal TX_CLK_CO. The more bursty the rate-altered clock signal, the larger the FIFO needs to be.

[0055] FIFO 70 uses the rate-altered clock signal TX_CLK_CO as a write clock and uses the smoothed upstream transmit clock TX_CLKA generated by feedback circuit 100 as a read clock.

[0056] Referring to Figure 6, feedback circuit 100 uses a phase locked loop 148 including a phase detector 150 that measures the differences between the clock signals TX_CLK_CO and TX_CLKA. This phase difference is either pre-filtered by a pre-filter 152 or immediately fed to a loop filter 154. The loop filter filters the output of the pre-filter (or the output of the phase detector in case no pre-filter is utilized) and generates an adaptive correction term (CW_LOOP) that is summed with a fixed fre-

quency control word, CW, by a summing circuit or algorithm 156. The sum of these two control words is fed into a numeric controlled oscillator (NCO) 158, which generates the upstream transmit clock signal TX_CLKA on a conductor 159. Additionally, NCO 158 is used to generate the phase information (μ) which is used by the variable interpolator 80 to interpolate data from the TX_CLKA domain to the TX_FS domain. The use of the phase information enables the relationship between the transmit clock signal (TX_CLKA) rate and sample signal (TX_FS) rate to be nearly arbitrary. In fact, the TX_CLKA rate and TX_FS rate must be related by some rational number, but in practice this allows a nearly unlimited choice of symbols rates with a fixed arbitrary sample rate.

[0057] To reduce the required circuit speed of loop filter 154, pre-filter 152 can be inserted at the output of phase detector 150, as shown in Figure 6. The pre-filter (which is a small circuit) must run at the same fast speed as the phase detector, while the loop filter may operate at a much lower frequency. The loop filter may be operated at the symbol clock (TX_CLK) rate instead of the sample clock

(TX_FS) rate, where TX_FS is the fast sampling clock and TX_CLKA is much slower. For example, TX_FS may be a 20 MHz clock, whereas TX_CLKA may be a 10 MHz clock.

[0058] Referring to Figure 7, an exemplary implementation of frequency divider 62 is shown which uses a counter-based architecture. The frequency divider comprises flip-flops 170 and 172, adders 174 and 176, a multiplexer (MUX) 178, a counter 180 and an exclusive OR gate 182. Many different types of frequency dividers may be used for divider 62. According to the Figure 7 embodiment, the input clock RX_CLK is divided by the ratio of the downstream transfer rate (ds-rate) and the upstream transfer rate (us-rate) to generate the rate-altered clock signal TX_CLK_CO. This clock is bursty. However, it has the same average frequency as the symbol clock 20 transmit signal. To generate the signal TX_CLK_CO, the sum of the ds-rate and us-rate is added to the signal sum_rate_next in case the difference of sum_rate_next and us-rate is negative, while the difference of sum_rate_next and us_rate is chosen by MUX 178 in case the difference is positive. Note that implementation in Fig. 7 is based on 2's

complement notation. However, the concept is not limited to this representation. Counter 180 counts RX_CLK clock cycles until the sum of the ds-rate and us-rate is reached and resets the output TX_CLK_CO. This can be done by XOR circuit 182, but the implementation is not limited to the use of an XOR gate.

[0059] Referring to Figure 8, phase detector 150 detects the rising edges of the two clocks TX_CLK_CO and TX_CLKA. An up/down counter 190 increments and decrements the counter every time a positive edge of the clock TX_CLK_CO and TX_CLKA is detected, respectively. The up/down counter can be initialized to a value m, which corresponds to half the size of FIFO 70 (Figure 3). Depending on the value (>m, =m or <m) of the counter, the outputs of the phase detector are set to their appropriate values by a comparator circuit 192 and are sent to pre-filter 152 (Figure 6). The embodiment of Figure 8 also includes registers 194-198 and NAND gates 200-201 connected as shown.

[0060] Referring to Figure 9, an exemplary embodiment of pre-filter 152 is illustrated, which reduces the required clock speed of loop filter 154. The inputs from the phase detector arrive at a clock speed of TX_FS and are accumulated in an accumulator 210. The output of the pre-filter can be saturated to any chosen bit-width. However, the smaller the number of output bits, the slower the clock exactly "synchronizes" to the rate-altered clock signal TX_CLK_CO. A slower clock like TX_CLKA can be used to latch the data to the loop filter. Pre-filter 152 also comprises registers 214-216 and an OR gate 218 connected as shown.

[0061] An exemplary embodiment of loop filter 154 is illustrated in Figure 10. Loop filter 154 receives the output of pre-filter 152 or the output of the phase detector 150 directly in case no pre-filter is used. Loop filter 154 filters the data received at its input. In general, there is no restriction on the order of the loop filter. In Figure 10, a second order loop filter is shown. The inputs are multiplied by the linear and integrator coefficients K0 and K1, respectively, in integrator multipliers 220 and 222. The outputs of the integrator

multipliers are fed into accumulators 224 and 226 and added to the outputs of the linear coefficient multipliers. Accumulator 226 cooperates with a register 228. The output of the loop filter from a register 230 is used as an additional input control word (CW_LOOP) to NCO 158.

[0062] Figure 11 illustrates an exemplary form of NCO 158. The output of the loop filter is fed to NCO 158 through summer 156 (Figure 6). The sum of the two control words CW and CW_LOOP is used to control NCO 158. In case an overflow in an accumulator 240 occurs, the most significant bit (msb) of a register 242 is set to one. This msb bit corresponds to the clock TX_CLKA while the phase information μ corresponds to the less significant bits of the output of the accumulator. For example, if register 242 is a 32 bit register representing bits 0-31, bit 0 corresponds to the msb and bits 1-12 correspond to phase information μ. The phase information is typically 8-12 bits in a 32 bit system.

While the invention has been described with reference to one or more preferred embodiments, those skilled in the

art will understand that changes may be made and equivalents may be substituted without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular step, structure, or material to the teachings of the invention without departing from its scope. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed, but that the invention will include all embodiments falling within the scope of the appended claims.